From Bruce Baller <baller@fnal.gov>
Sent Thursday, February 28, 2008 8:03 am
To bromberg@pa.msu.edu
Cc Dan Edmunds <edmunds@pa.msu.edu> , Stephen Pordes <stephen@fnal.gov> , Mitchell Soderberg <mitchell.soderberg@yale.edu>
Subject Re: DSP
Attachments FFT.xls 1.2MB

Carl,

This is a nice segue into what I have been doing the past few days. The attached spreadsheet shows the effect of the preamp and shaper electronics on garfield signals along with some coherent noise, and method for decoding the ADC's.

I use the Excel FFT macro to convolute the wire signals & noise with the preamp and shaper electronics in columns K - Q, then deconvolute the convoluted signal in columns S - W. The rms error between the original signal and the deconvoluted signal is shown in column X. Power spectrum calculations are in columns Z - AC.

There are 2 Wire Signal columns so that you can overlap hits.

I added a significant noise term at 400 kHz in this example and then applied a notch filter (See cells U85 - U87) to remove the noise term. The "Coll Chart" chart shows the results.

You can run the FFT macro by clicking on the "Do FFT" button. You need to ensure that you have loaded the AnalysisPak add-in first (Under the Tools/Add-ins menu). You can change the noise amplitude and frequency in cells E2 and F2.

BTW, if you add or remove columns or cells you will have to edit the macro. Also note that the character strings "FFT_" and "InvFFT_" in row 2 are directives to tell the macro the data source column for the FFT.

I am convinced that this will be the best way to decode the ADC's.

Carl Bromberg wrote:
> Hi Guys:
>
> You may already know all about this, but I think the following link
> has everything we need to know to extract the signal (time, amplitude,
> width, etc.) for a hit on a track from the digitized output of the PFC
> modules.
>
> http://www.dspguide.com/
>
> I wish I had the time to lock myself in a room for a week (maybe a
> month) to digest it. Then comes the programming.
>
> A good project for a graduate student would be to implement a simple
> algorithm for the FPGA in the ADF-2.
>

> Best regards,
> Carl